Exhibit 59

No. 21-1772

United States Court of Appeals for the Federal Circuit

ACQIS, LLC,

Plaintiff-Appellant,

– v. –

EMC CORPORATION,

Defendant-Appellee.

On appeal from the United States District Court
for the District of Massachusetts, No. 1:14-cv-13560-ADB,
Hon. Allison Dale Burroughs

CORRECTED BRIEF FOR PLAINTIFF-APPELLANT

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U.S. Patent No. RE43,171 (Claim 24)

24. A method comprising: providing a computer module, the module comprising

a central processing unit,

a connection program,

an integrated interface controller and bridge unit to output an encoded serial bit stream of **address and data bits of [a] Peripheral Component Interconnect (PCI) bus transaction,** the integrated interface controller and bridge unit coupled to the central processing unit without any intervening PCI bus, and

a low voltage differential signal channel coupled to the integrated interface controller and bridge unit to convey the encoded serial bit stream of PCI bus transaction,

inserting the computer module into a computer console, the computer console having access to a network,

receiving connection information from the computer console,

configuring the connection program to adapt to the connection information, and

establishing a connection between the computer module and a server coupled to the network,

wherein the low voltage differential signal channel further comprises two sets of unidirectional serial bit channels which transmit data in opposite directions.

(Disputed text emphasized)

CERTIFICATE OF INTEREST

Pursuant to Federal Circuit Rule 47.4, counsel for Plaintiff-Appellant, certifies the following:

1. The full name of the party represented by me is ACQIS LLC.

2. The name of the real party in interest (if the party named in the caption is not the real party in interest) represented by me: N/A.

3. Parent corporations and publicly held companies that own 10% or more of stock in the party: ACQIS Technologies, Inc.

4. The names of all firms and the partners or associates that appeared for the party now represented by me in the trial court or are expected to appear in this Court (and who have not or will not enter an appearance in this case) are:

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   Brian Eutermoser (King & Spalding LLP)
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5. The title and number of any case known to counsel to be pending in this or any other court or agency that will directly affect or be directly affected by this court's decision in the pending appeal:

    - *ACQIS LLC v. Samsung Elecs. Co., et al.*, No. 2:20-cv-00295 (E.D. Tex.);
    - *ACQIS LLC v. Acer Inc.*, No. 2:21-cv-00275 (E.D. Tex.);
    - *ACQIS LLC v. MITAC Holdings Corp., et al.*, No. 6:20-cv-00962 (W.D. Tex.);
    - *ACQIS LLC v. Inventec Corp.*, No. 6:20-cv-00965 (W.D. Tex.);
    - *ACQIS LLC v. Asustek Comput., Inc.*, No. 6:20-cv-00966 (W.D. Tex.);
    - *ACQIS LLC v. Lenovo Grp. Ltd., et al.*, No. 6:20-cv-00967 (W.D. Tex.);
    - *ACQIS LLC v. Wistron Corp., et al.*, No. 6:20-cv-00968 (W.D. Tex.).

6. The organizational victims and bankruptcy cases applicable to this appeal: N/A.

Dated: August 16, 2021

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STATEMENT OF RELATED CASES

Pursuant to Federal Circuit Rule 47.5, Appellant ACQIS, LLC states that the following is a list of related cases:

- *ACQIS LLC v. Samsung Elecs. Co., et al.*, No. 2:20-cv-00295 (E.D. Tex.);
- *ACQIS LLC v. Acer Inc.*, No. 2:21-cv-00275 (E.D. Tex.);
- *ACQIS LLC v. MITAC Holdings Corp., et al.*, No. 6:20-cv-00962 (W.D. Tex.);
- *ACQIS LLC v. Inventec Corp.*, No. 6:20-cv-00965 (W.D. Tex.);
- *ACQIS LLC v. Asustek Comput., Inc.*, No. 6:20-cv-00966 (W.D. Tex.);
- *ACQIS LLC v. Lenovo Grp. Ltd., et al.*, No. 6:20-cv-00967 (W.D. Tex.);
- *ACQIS LLC v. Wistron Corp., et al.*, No. 6:20-cv-00968 (W.D. Tex.).

INTRODUCTION

ACQIS is a pioneer in modular computing. A "modular" computer consists of computer "modules" attached to a shared "console." Each module contains the core elements of a computer, and the console provides modules access to shared resources.

ACQIS invented a technique for connecting modules to the consoles using a new "interface channel" that was faster, more efficient, and less costly than existing channels, but still compatible with existing software because it could still communicate the "transactions" defined by the dominant communication standard of the time—the "Peripheral Component Interconnect" Standard ("PCI Standard").

To protect this invention, ACQIS obtained the eight asserted patents, which belong to three patent families. *See* Appx2495–2498 (¶¶ 95–97) (illustrating family relationships). Each claims a computer module employing the new interface channel to transmit at least some portion of a "PCI bus transaction" between a processor and peripheral device.

The PCI Standard was succeeded by the "PCI Express" standard ("PCIe"), which adopted the same new interface channel ACQIS invented.

EMC makes and sells computer modules that use PCIe to connect processors to peripheral devices. ACQIS filed suit because those EMC computer modules use the claimed interface channel to communicate "PCI bus transactions."

After over a decade of litigation—in which the first district court to consider the issues construed the claims in ACQIS's favor and the PTAB upheld all of ACQIS's claims—the district court granted EMC summary judgment of non-infringement against all asserted claims on the basis that PCIe does not communicate "PCI bus transactions," as construed by the district court.

That was error for three reasons. First, the district court erroneously refused to consider ACQIS's arguments about the meaning of "PCI bus transaction" as supposedly untimely. Second, the district court's construction of that phrase was wrong. Third, its construction of "PCI bus transaction" does not support summary judgment of non-infringement against *all* asserted claims. Because the district court granted summary judgment against all claims based on these errors, the Court should reverse and remand.

STATEMENT OF JURISDICTION

The United States District Court for the District of Massachusetts had jurisdiction over this case pursuant to 28 U.S.C. §§ 1331 and 1338(a). It entered final judgment through an Order of Dismissal on February 19, 2021. Appx14, Appx3558. Appellant timely filed a notice of appeal on March 19, 2021. Appx3559. This Court has jurisdiction pursuant to 28 U.S.C. § 1295(a)(1).

STATEMENT OF THE ISSUES

1. Whether the district court erred by (a) declining to consider ACQIS's claims based on an erroneous finding of waiver, (b) granting summary judgment of non-infringement based on a fundamentally flawed construction of "PCI bus transaction," and (c) doing so even as to claims that recited communicating only the "address and data bits" of a transaction that the court construed such a transaction to require.
2. Whether the district court misconstrued "communicating … a PCI bus transaction" based on an apparent agreement between the parties that did not exist.
3. Whether the district court misconstrued "encoded ... (PCI) bus transaction" based on a prosecution disclaimer that had not occurred.

STATEMENT OF THE CASE

A. Technology Background

The primary question on appeal is what information constitutes a "PCI bus transaction." According to ACQIS, a PCI bus transaction is the information exchanged between PCI components. According to EMC and the district court, a transaction is that information *plus* signals for controlling the physical medium over which that information used to be exchanged. Deciding this issue requires understanding (1) the PCI Standard, (2) improvements claimed in the asserted patents, and (3) the PCIe standard.

1. PCI Standard

Computer processors communicate with peripheral devices such as mice, keyboards, and graphics cards. In the 1990s, the "most widely accepted and implemented [peripheral device communication] standard in the world" was the PCI Standard. Appx2466–2473 (¶¶ 42–57). That standard was published in the 1992 "PCI Local Bus Specification" ("PCI Specification"). Versions 2.1 and 2.2 followed in 1995 and 1998. Appx2236; Appx2467–2468 (¶¶ 45-47); *see* Appx2235–2359.

The PCI Standard defines (1) a "transaction" layer and (2) a "physical layer." Appx2469 (¶ 48). The "transaction layer" defines the messages ("transactions") that PCI components communicate. The "physical layer" defines the physical infrastructure that communicates those transactions and signals used to control that physical infrastructure. *Id.* Analogizing to a telephone call, the transaction layer defines the content of a telephone conversation (*i.e.*, the message), whereas the physical layer defines both the telephone network's physical infrastructure and the signals for controlling that infrastructure (*i.e.*, signals for establishing and maintaining a connection).

a) PCI Transaction Layer

PCI components communicate by exchanging PCI "transactions." *See* Appx1205–1207 (¶¶ 61–66). Those transactions are "the information

conveyed" between two PCI components. Appx2505 (¶ 110); *see also* Appx1205 (¶ 61).

A "transaction" is conveyed in at least two phases: "an address phase followed by one or more data phases." Appx2246 (footnote omitted); *see also* Appx2470 (¶ 50). A "phase" is a time period "in which a single unit of information is transferred." Appx3396–3397 (¶ 18). Data transferred in paired address and data phases typically include (1) "command bits," (2) "address bits," (3) "data bits," and (4) "byte enables." *See* Appx1205 (¶ 61); Appx3397 (¶¶ 19–20).

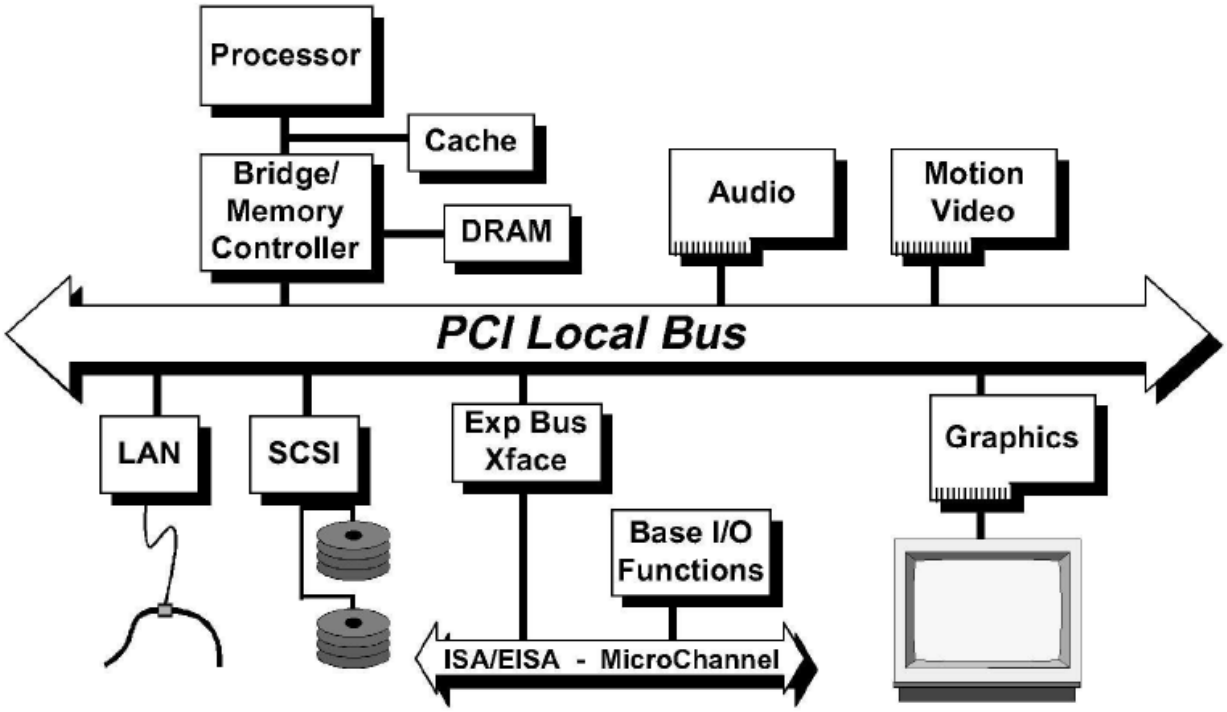
During the "address phase," the devices exchange: (1) "command bits" and (2) "address bits." Appx2470, Appx2472 (¶¶ 51, 54). "Command bits" indicate what PCI command is being performed. Appx2470, Appx2505 (¶¶ 50, 110); Appx1205 (¶ 61). Example commands include reading data from (or writing data to) a given location in memory. Appx2470, Appx2505 (¶¶ 50, 110); Appx1205 (¶ 61). The "address bits" indicate the memory locations (*i.e.*, memory "addresses") that the command targets. Appx2470, Appx2505 (¶¶ 50, 110). For example, if the command is to write data, the "address bits" indicate the memory address to write to. Appx2470 (¶ 50). For different types of commands, the PCI Standard defines different formats for the address bits, as well as different "address spaces" (*i.e.*, reserved areas of memory) where the commands operate. Appx2470–2471, Appx2585 (¶¶ 51, 220).

"[D]ata phases" follow "address phase[s]." Appx2472–2473 (¶ 56). During data phases, the PCI components exchange two types of information: (1) "data bits" and (2) "byte enable[s]." *Id.* The data bits indicate the data for the transaction. *Id.* For example, if the command was to write data in the address phase, then the data bits are the data to write to the memory address also identified during that address phase. *Id.* The "Byte Enables" indicate which of the data bits are used. Appx2246. Thus, the transaction layer specifies the information to be communicated, the address, and the operation.

b) PCI Physical Layer

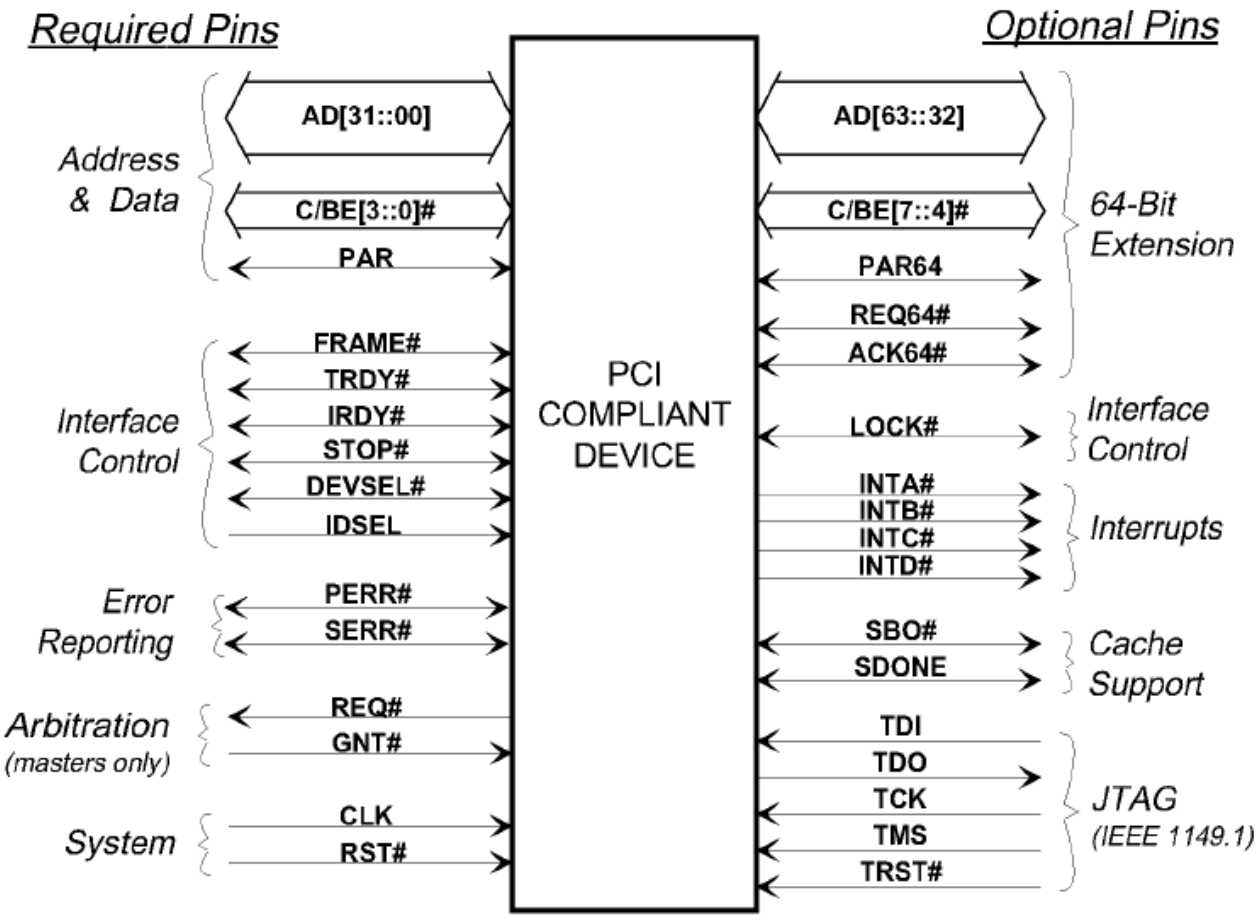
Whereas the "transaction layer" defines the information communicated, the PCI Specification's "physical layer" defines (1) the physical infrastructure that communicates transactions and (2) signals that coordinate this communication across that physical infrastructure. Appx2469 (¶¶ 48–49).

The figure below shows an example system's physical infrastructure using the PCI Standard.



Appx2240. This figure shows a processor and peripheral devices (*e.g.*, audio, video, and graphics cards) connected to the bus. Appx1204–1205 (¶ 58–60). The salient physical feature of the PCI Standard is the "PCI Local Bus"—a physical broadcast medium to which the PCI components connect and through which they exchange transactions. Appx2466–2473 (¶¶ 42–57).

The diagram below details the physical "interface" (*i.e.*, the wiring) by which components connects to the PCI Local Bus. Appx2469 (¶ 49).



Appx2469 (¶ 49). The left hand shows the "Required Pins" (*i.e.*, wires) for connecting to the bus, and the right side shows optional pins. As shown, at least 47 "pins" are required of all components and another two for components that initiate transactions ("masters"). Appx2469 (¶ 49).

Thirty-two "AD" ("address and data") pins and four "C/BE" ("command and byte enable") pins transmit the address, data, command, and byte enable bits described above. Appx2246. During the address phase, the 32 AD pins ("AD[31::00]") transmit 32 address bits, and the four C/BE pins ("C/BE [3:00]#") transmit four command bits, one bit across each pin in parallel, *i.e.*, simultaneously. Appx1854–1855 (¶ 140). During subsequent

data phases, the 32 AD pins transmit the 32 data bits, and the four C/BE pins transmit the four byte enables. Appx1854–1855 (¶ 140). The bits transmitted on the four C/BE pins (*i.e.*, "command" in the address phase and "byte enables" in the data phases) are referred to as the "control bits" because they control what the target PCI component does with the data it receives. Appx2473, Appx2599 (¶¶ 57, 239); Appx3419–3420 (¶ 83).

The remaining 13 required pins control transmission of the transaction. Appx3399 (¶ 26). For example, two "arbitration" pins obtain control of the physical parallel PCI bus. Appx3399–3400 (¶¶ 26–27); *see also* Appx1854–1855(¶ 140). Six "Interface Control" pins coordinate communication of the transaction over the physical parallel PCI bus—*e.g.*, by indicating which device is the recipient (DEVSEL#), when it is ready to receive the transaction (IRDY# and TRDY# signals), and when a transaction starts and ends (FRAME# signals). Appx1854–1855 (¶ 140). Additional signals control timing (CLK), detect and report transmission errors on the physical parallel PCI bus ("PAR", SERR#, and PERR#), and reset (RST#). Appx1854–1855 (¶ 140).

2. Patented Technology

The asserted patents concern modular computers that communicate at least some portion of a "PCI bus transaction" between a processor and a peripheral device. Appx2498–2501 (¶¶ 98–102).

Each module contains the core elements of a computer (*e.g.*, processor, memory), and shared consoles provide those modules with access to shared peripheral devices (*e.g.*, I/O devices, mass storage devices, *etc.*). *Id.* Modular computers are popular in data centers, which arrange thousands of computer servers on "racks" that provide shared peripherals. Appx2463–2464 (¶¶ 35–38).

a) The Problem: Backwards Compatibility

In the 1990s, ACQIS recognized that the demand for data centers would grow exponentially and that modular computers could lower data center costs, reduce space requirements, improve energy efficiency, and ease maintenance. Appx2490–2491, Appx2498, Appx2500–2501 (¶¶ 84, 98, 102). But making modular computing feasible in these environments required confronting the PCI Standard's shortcomings. Appx2501 (¶ 103).

At the time, "the ability to execute a PCI bus transaction was required for a computer system to be commercially acceptable." Appx2501 (¶ 103). But the PCI Standard's *physical layer* was ill-suited for modular computing. Appx2501 (¶ 103). The 47-pin connections were too cumbersome for densely packed data centers (Appx37 (3:35-49); Appx2462, Appx2463–2464 (¶¶ 32, 36–38)), expensive, and energy inefficient (Appx37 (3:35); Appx2501 (¶ 122)). Moreover, such connections were slow: the "shared bus topology," which required that "only one device can 'talk' at any one time," is ill-suited for connecting a large number of components. Appx2512 (¶¶ 121–22). And

so many wires in "parallel" created reliability issues (due to electromagnetic interference and signal "skew"), exacerbated by the long cable lengths required. Appx2464–2465 (¶ 39); Appx37 (3:64–65). These issues made it impractical for ACQIS to connect modules to consoles using PCI buses. Appx2502 (¶ 105).

Nevertheless, ACQIS could not abandon the PCI Standard because "the ability to execute a PCI bus transaction was required for a computer system to be commercially acceptable." Appx2501 (¶ 103). Accordingly, ACQIS had to overcome these problems while still supporting the Standard.

b) ACQIS's Solution.

ACQIS solved the problem by replacing parallel buses with *serial* interface channels—specifically, "low voltage differential signal" ("LVDS") channels—that maintained backwards compatibility with the PCI Standard. Appx37 (3:64-65) Appx38 (5:31-62); Appx2503 (¶ 107). "Serial" channels send data one bit at a time, as opposed to "parallel" channels, which send multiple bits, "in parallel" (*i.e.*, simultaneously). Appx2464–2466 (¶¶ 39–41). ACQIS replaced the parallel PCI bus with a new serial interface channel that used far fewer pins/wires and thus mitigated the bulk, cost, energy, and performance shortcomings of the PCI Standard's physical layer. Appx38 (5:31–62).

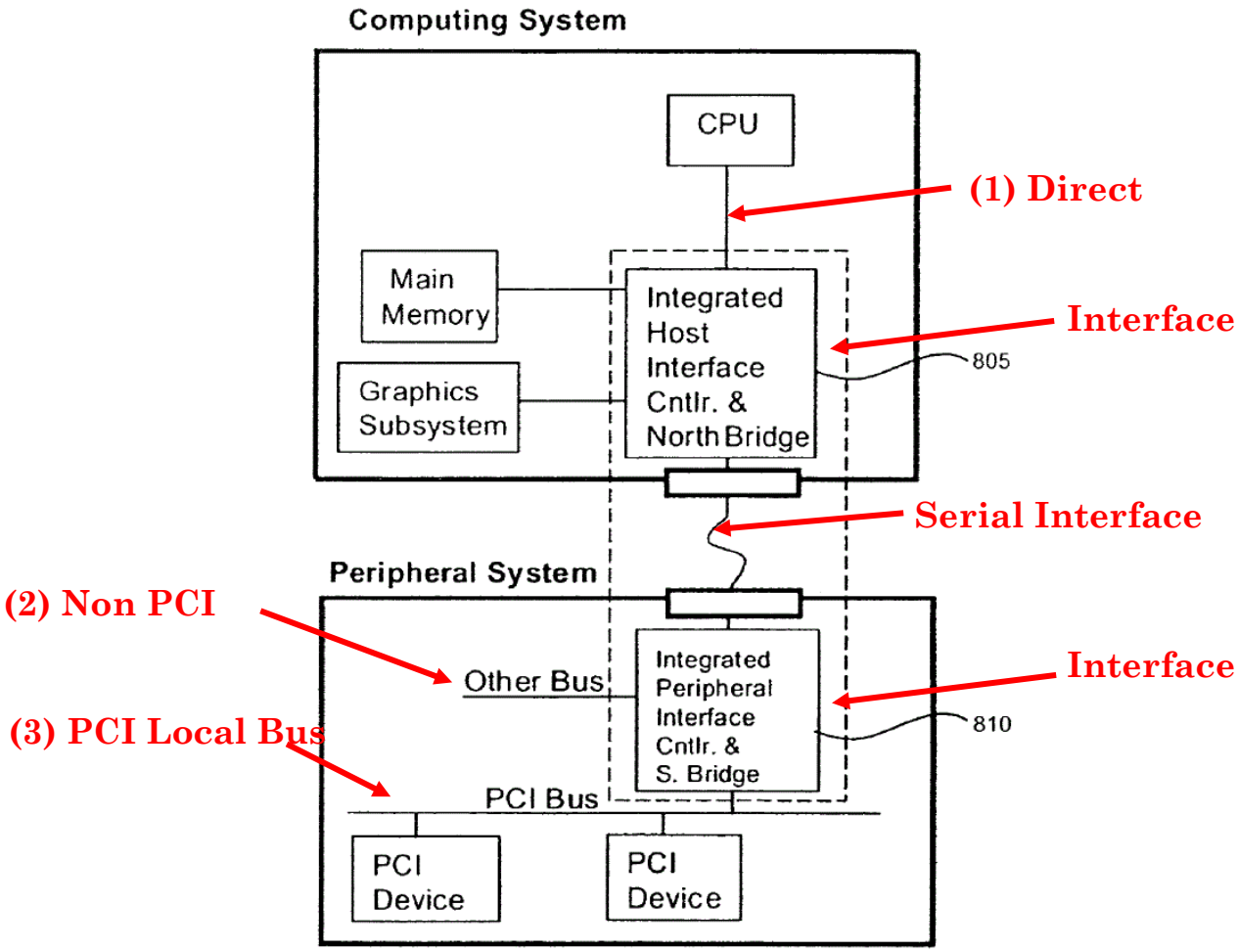
ACQIS added "interface controllers" that enabled the serial interface channel to communicate the same PCI transactions defined by the PCI

Standard and therefore remain compatible with existing PCI software. Appx2491 (¶ 85). The interface controllers included "translators" for encoding and decoding PCI data received from PCI components, a "transmitter" for transmitting encoded data on the new serial channel, and a "receiver" for PCI data from the serial interface channel. Appx38 (6:37-49). In addition, for some applications, ACQIS integrated the serial interface channel directly into a processor.

Thus, ACQIS replaced the PCI Standard's physical layer (including the parallel PCI Local Bus) with this combination of serial interface channels and interface controllers, yet it maintained backwards compatibility by enabling the new physical layer to communicate PCI Standard bus transactions.

c) Asserted Patents

The eight asserted patents each disclose a modular computer that communicates at least some part of a "PCI bus transaction" over serial interface channels. For example, Figure 8 of the '415 Patent is a block diagram showing a "Computing System" (computer module) and a "Peripheral System" (console), connected by a serial interface channel. As shown, access to that channel is controlled on either end by an "interface controller."



'415 Patent (Fig. 8) (annotations in red).

PCI components connect to interface controllers any way, such as by using a (1) Host CPU Bus, (2) non-PCI bus, or (3) PCI Local Bus. In Figure 8, the CPU connects *directly* to the "host interface controller" (805) whereas "Peripheral System" components connect to the "peripheral interface controller" (810) through a legacy PCI Local Bus or "other bus." Appx44 (17:65-67) (serial interconnect "may be used to interface … PCI-like buses").

Where the PCI components connect to the interface controller using a PCI Local Bus (*e.g.*, Figure 7 of the '415 patent), the interface controllers

capture and communicate *both* PCI transaction *and* PCI physical layer signals so those signals may be recreated on the receiving end. '415 Pat. (16:48-54, 20:43-48). Physical layer signals are captured and processed using different hardware than the transaction data. '415 patent (17:16-54). For example, a "control encoder" reads the parallel control signals from the PCI Local Bus, records them in memory as additional "control bits," and passes them to a "transmitter" for transmission across the serial interface channel. '415 patent (17:35-41). At the transmitter, the control bits in memory are "serialized by parallel to serial converters" (*e.g.*, grouped into 10-bit packets) and transmitted across the serial interface channel. '415 patent (18:1-7).

d) Asserted claims

Each asserted claim recites a modular computer system that uses interface controllers to communicate at least some part of a "PCI bus transaction" across a serial interface channel. Seven claims recite that the controllers communicate the entire "(PCI) bus transaction"[1] or the "data of … [a] (PCI) bus transaction."[2] Four recite that the controller communicates

[1] '873 patent (cls. 29 and 61) (Appx163, Appx165); '294 patent (cl. 44) (Appx195).

[2] '416 patent (cl. 60) (Appx52); *see also* '487 patent (cls. 38 and 49) (Appx104, Appx105) ("bus transaction data").

only the "*address and data bits* of a … (PCI) bus transaction" (the "Address and Data Claims").[3]

Each of those Address and Data Claims recites that the CPU connects to the controller "*without any intervening PCI bus*." Claim 24 of the '171 patent is one such example:

> 24. A method comprising: providing a computer module, the module comprising
>
> a central processing unit,
>
> a connection program,
>
> an integrated interface controller and bridge unit to output an encoded serial bit stream of **address and data bits of [a] Peripheral Component Interconnect (PCI) bus transaction,** the integrated interface controller and bridge unit coupled to the central processing unit **without any intervening PCI bus**, and
>
> a low voltage differential signal channel coupled to the integrated interface controller and bridge unit to convey the encoded serial bit stream of PCI bus transaction,
>
> inserting the computer module into a computer console, the computer console having access to a network,
>
> receiving connection information from the computer console,

[3] '171 patent (cl. 24) (Appx332); '468 patent (cl. 29) (Appx372); '814 patent (cl. 31) (Appx246); '119 patent (cl. 38) (Appx293) ("('PCI') bus transaction address and data").

configuring the connection program to adapt to the connection information, and

establishing a connection between the computer module and a server coupled to the network,

wherein the low voltage differential signal channel further comprises two sets of unidirectional serial bit channels which transmit data in opposite directions.

Appx332 (emphasis added).

3. PCIe Standard

In 2002, PCI Express succeeded the PCI Standard. Appx2473–2474 (¶ 59). "One of the most important design goals for PCIe was backward compatibility with PCI software." Appx2476–2478 (¶ 63). To achieve compatibility, "PCI Express maintain[ed] the same standard transactions defined in the PCI Local Bus Specification." Appx2479 (¶ 65). That is, PCIe defined "transactions" "using PCI standard addresses, data, encoded commands, and byte enables." Appx2479–2484 (¶¶ 65–73). By maintaining the same transaction layer as PCI, PCIe was "100-percent compatible with conventional PCI compliant operating systems and their … software." Appx2476–2478 (¶ 63).

While retaining the PCI Standard's transaction layer, PCIe replaced the *physical* layer. Appx2481 (¶ 68). Specifically, just as ACQIS had before,

it replaced the physical PCI Local Bus with a serial LVDS channel. Appx2473–2475 (¶¶ 59–61).

Thus, as ACQIS had, the PCIe standard ensured that "[k]ey PCI attributes, such as its usage model, load-store architecture, and software interfaces, are maintained, whereas its bus implementation is replaced by a highly scalable, fully serial interface." Appx1781 (¶ 51).

B. Procedural Background

EMC makes and sells modular computers using PCIe. Appx1774 (¶ 4). Those systems infringe because they use the claimed serial interface channel to communicate "PCI bus transactions."

1. Eastern District of Texas

On September 9, 2013, ACQIS filed an infringement suit against EMC in the Eastern District of Texas, which was assigned to Judge Davis. Appx2. After EMC moved to transfer to Massachusetts, Judge Davis agreed, but only after claim construction. Appx2.

After briefing and a *Markman* hearing on February 21, 2015, as relevant here, Judge Davis construed the phrases (1) "PCI bus transactions" and (2) "encoded ... PCI bus transactions."

a) "PCI bus transaction"

The parties agreed that a "PCI bus transaction" refers to a transaction as defined in the PCI Standard, but disagreed over whether such a transaction must be "communicated over a PCI bus." Appx505. This was a potentially dispositive non-infringement issue because the accused devices do not have PCI Local Buses.

ACQIS contended that no PCI Local Bus was required because a "PCI bus transaction" was the transaction layer "*information* content according to the PCI standard" (*i.e.*, the "command, address, and data" bits) and this information could be created *without* a PCI Local Bus. Appx390–395.

Judge Davis agreed with ACQIS and construed "PCI bus transaction" as "information, in accordance with the PCI standard, for communication with an interconnected peripheral component." Appx506–507 (quotation marks omitted). He did not detail that information other than by referring to the Standard.

b) "encoded … PCI bus transaction"

EMC argued that the claims require the "PCI bus transaction" to be "encoded," and "encoding" means converting the transaction from parallel signals into bits for transmission on the serial interface channel. Appx454. EMC planned to argue that, because its products lack a PCI bus, the

"transactions" communicated do not start as parallel signals and therefore are never converted into bits for serial transmission.

Judge Davis rejected that argument too. He held that "an encoded PCI bus transaction does not require any parallel-to-serial conversion at all," and that an "encoded" transaction is merely "code representing a PCI bus transaction." Appx508; *see also* Appx390–398 (ACQIS arguing for this construction).

2. Patent Trial and Appeal Board

The District of Massachusetts stayed the litigation pending resolution of IPRs EMC had filed against claims 54 and 56-61 of the '873 patent (Appx1091) and claims 24 and 31-33 of the '814 patent (Appx1066). Appx3.

The parties again disputed the meaning of "PCI bus transaction" and "encoded … PCI bus transaction."[4] This time, EMC changed positions.

a) "PCI bus transaction"

EMC now argued that a "PCI bus transaction" meant any "communication with an interconnected peripheral component," without regard to the PCI Standard. Appx550. ACQIS again argued that a "PCI bus transaction" is the "command, address, and data information, in accordance with the [transaction layer of the] PCI standard." Appx679, Appx673–685.

[4] "Communicating … a PCI bus transaction" was not at issue.

The Board rejected EMC's argument, holding that a "PCI bus transaction" "refers to a particular industry standard, not to just any communication with an interconnected peripheral component." Appx1094–1096. It therefore construed "PCI bus transaction" as a "(PCI) industry standard bus transaction." Appx1094–1096. Like Judge Davis, the Board did not specify what the Standard requires. Appx1094–1095.

b) "encoded … PCI bus transaction"

EMC also changed its tune on the "encoded" limitation, arguing that an "encoded" transaction simply means "converted or formatted from one form into another." Appx972–973.

ACQIS argued that "encoded" meant certain reversible operations, including those that "(1) turn[] a signal into bits, (2) group[] bits into a specified size block, or (3) order[] bits onto one or more serial transmission lines." Appx797–799. ACQIS emphasized that the definition does *not* require that the transaction begin as parallel signals. Appx1047 (50:12-22) (ACQIS arguing that it does not "matter where [the data] originates from").

The Board did not construe this term because ACQIS *conceded* that the cited art "encoded" transactions under ACQIS's construction—specifically, by using "8b/9b line encoding," which groups bits into specified size blocks. Appx817. EMC agreed to the concession and therefore argued

that the Board "need not construe 'encoded.'" Appx972–973. Consequently, *neither* party advocated a construction of "encoded" requiring a transaction to start as parallel signals. *See also* Appx1752 (¶ 57) (EMC arguing that such encoding "is not parallel-to-serial conversion.")

c) Final Written Decision

The Board upheld all challenged claims. After accepting ACQIS's concession that the prior art's "8b/10b line encoding" satisfies the "encoded" limitation (Appx1099–1100, Appx1104 n.4), it still found no invalidity because the prior art (*e.g.*, "Horst") failed to communicate "PCI bus transactions." Appx1099–1103. Rather, the prior art transmitted "TNet" transactions, which the Board held do not include "*any* address bits" or "*any* data bits" "of a PCI industry standard bus transaction," Appx1100–1101 (emphasis added), exactly ACQIS's argument. Appx1099–1103; Appx815, Appx820; *see also* Appx782, Appx793, Appx795, Appx801, Appx806, Appx808.

3. Subsequent District Court Claim Construction

After the stay was lifted, EMC argued that "critical developments during the IPRs" required the district court to revisit the constructions of (1) "PCI bus transaction," (2) "encoded … PCI bus transaction," and (3) "communicating … [a] PCI bus transaction." Appx1121. According to

EMC, ACQIS had purportedly disclaimed its litigation positions with respect to these three terms at the IPR hearing. It had not.

a) "PCI bus transaction"

EMC urged the district court to reconsider the construction that "PCI bus transaction" does not require a PCI bus. Appx506–507. According to EMC, ACQIS purportedly disclaimed that construction by telling the Board that the absence of a PCI Local Bus in Horst is "one indicator" that Horst does not communicate PCI transactions. Appx1130–1131; Appx1043–1044.

The district court rejected that argument because ACQIS in fact had told the Board that "the claims don't require a bus," that the absence of a PCI bus in Horst was simply "one indicator," and this indicator was "not determinative." Appx1700–1704, Appx1707 (citing Appx3580–3581); *see also* Appx1043–1044 ("You don't have to have the PCI bus" because "[y]ou could generate a PCI transaction without a bus").

The district court then construed "PCI bus transaction" consistently with Judge Davis's construction: a "transaction, in accordance with the industry standard PCI Local Bus Specification, for communication with an interconnected peripheral component." Appx1703–1704. Again, the district court did not say what information a "PCI bus transaction" must include to be "in accordance with the … Specification." Appx1704.

b) "encoded … PCI bus transaction"

EMC urged the district court to revisit Judge Davis's construction that "encoded" "does not require any parallel-to-serial conversion at all." Appx508. According to EMC, ACQIS's IPR arguments limited an "encoded … PCI bus transaction" to one that had undergone parallel to serial encoding. Appx1136–1137.

ACQIS protested that it "never took the position that encoding required parallel-to-serial conversion." Appx1175; *see* Appx1167–1170, Appx1173–1177. To the contrary, ACQIS had explicitly asked the Board to construe that term more broadly (Appx1168–1170, Appx1173–1175; *see also* Appx797–799), and it *conceded* that the prior art "encoded" based on that broader construction (Appx817; *see* Appx1099–1100, Appx1104 n.4).

Nevertheless, based on ACQIS's statements at the hearing describing the importance of transmitting a transaction in serial form, the court held that ACQIS had "clearly and unmistakably" argued that "an encoded PCI bus transaction requires that a PCI bus transaction be encoded for serial transmission *from a parallel form*,". Appx1704–1711 (emphasis added). The district court reached that incorrect conclusion because it misunderstood ACQIS's emphasis on communicating data in *serial* form to imply that the data must have started in *parallel* form.

Based on this purported disclaimer, the district court construed "encoded … PCI bus transaction" as "a PCI bus transaction that has been serialized *from a parallel form*." Appx1711.

c) "communicating … [a] PCI bus transaction"

EMC raised a new dispute concerning "communicating … [a] PCI bus transaction." Appx1137. EMC argued that, due to purported IPR disclaimer, that phrase meant "communicating a PCI bus transaction, including *all address, data and control bits, without discarding any of those bits*." Appx1137 (emphasis added).

But ACQIS had never argued that the accused products communicate any less than an entire PCI bus transaction. Indeed, ACQIS's position was that "communicating" simply carried its ordinary meaning, and any dispute over what "communicating … [a] PCI bus transaction" means would be resolved by construing "PCI bus transaction." Appx1147; *see also* Appx1177–1178; Appx1413; Appx1635 (220:1–5), Appx1642 (227:19-25).

Consequently, ACQIS agreed at the *Markman* hearing that "communicating … [a] PCI bus transaction" means communicating "all address, data and control bits," *provided that "control bits" refers to the command information*. Appx1643 (228:2–15) ("I think that's right. Because I think you would communicate … the address, *you do communicate a*

command that tells you what you have to do and then you send the data. So I think that's right. That's all right") (emphasis added); *see also* Appx1643 (226:12–15) ("control bits … refer[s] to the command" information). The court then adopted that construction pursuant to the agreement. Appx1711.

The parties did not agree on a construction for the related phrase "communicate *address and data bits of* [a] PCI bus transaction," and similar variations, as recited in the Address and Data Claims. ACQIS argued that these claims could not require transmitting the address and data bits *and also the control bits*, because that would contradict those claims' language. Appx1177–1180; Appx1635–1636 (220:15–221:6), Appx1637 (222:14–23).

ACQIS disputed having made any IPR disclaimer regarding the Address and Data Claims. Appx1176–1180. Rather, as ACQIS pointed out, the quotations EMC had cited to support its disclaimer argument dealt with ACQIS defining a "PCI bus transaction" generally or the requirements of claims other than the Address and Data Claims. Appx1177–1180.

4. Summary Judgment

EMC moved for summary judgment of non-infringement based on each of those three constructions.

a) "PCI bus transaction" / "communicating … PCI bus transaction"

EMC primarily argued that the accused products do not communicate a "PCI bus transaction" because they do not communicate certain *physical layer signals*. Appx6–11, Appx12–13. According to EMC, both (1) a "transaction, in accordance with the … PCI Local Bus Specification" and (2) "communicating … control bits" require communicating certain physical layer signals, including the "interface control signals" and the "parity bit." Appx1735–1736, Appx1738, Appx1764–1767. EMC argued that the accused products have no PCI Local Bus and therefore do not use these physical layer signals. Appx1735–1736.

ACQIS protested that the PCI Local Bus Specification requires only information for the *transaction layer*, and not the information described by the physical layer. Appx3347–3359, Appx3373–3376. Moreover, it argued that "control bits" refers only to the "command bits," as ACQIS had made explicit at the *Markman* hearing. Appx3345–3347, Appx3347–3359.

ACQIS also argued that, even if a "transaction" requires these physical layer signals, summary judgment would still be inappropriate against the Address and Data Claims, which explicitly recite transmitting only the "address and data bits of a PCI bus transaction." Appx3337–3338.

Finally, ACQIS argued that genuine fact disputes remained about whether PCIe communicates signals analogous to the disputed physical layer signals. Appx3373, Appx3376–3378; Appx3386–3388 (¶¶ 15–19, ¶ 21).

b) "encoded … PCI bus transaction"

EMC also sought summary judgment of non-infringement because PCIe does not serialize PCI bus transactions *from parallel form*, as required by the district court's construction. Appx1756.

ACQIS responded that as ACQIS's expert had opined, "PCI Express data *is* … sent to the parallel-to-serial converter for serialization before transmission over the serial PCI Express channels." Appx3370–3372 (emphasis added). Thus, a genuine dispute of material fact barred summary judgment.

Summary Judgment Order

Two and a half years later (and without oral argument), the district court granted EMC summary judgment of non-infringement. Appx1–13.

Although the 13-page order discussed each of EMC's three arguments, its reasoning turned only on the court's *reinterpretation* of "PCI bus transaction": the district court (1) agreed with EMC that a "transaction, in accordance with the … PCI Local Bus Specification" means information that includes the physical layer's "control" and "parity" signals (Appx6–11), and

it held that, because the accused products lack a "PCI bus transaction," they cannot (1) "communicat[e] … [a] PCI bus transaction" or (2) "encode[] … [a] (PCI) bus transaction" (Appx11–13).

The district court dismissed ACQIS's counterarguments as "untimely" "attempt[s] to reopen claim construction." Appx9. It refused to consider those arguments because "district courts are not obligated to rule on claim construction arguments presented for the first time in summary judgment briefs." Appx9–10.

The court never reached ACQIS's separate arguments regarding the Address and Data Claims, which recite transmitting only the address and data bits of the transaction rather than an entire transaction. Nor did it reach ACQIS's argument that genuine fact disputes remained about whether PCIe communicates signals analogous to the disputed physical layer signals.

SUMMARY OF THE ARGUMENT

The district court erred by granting summary judgment of non-infringement based on a new and incorrect construction of "PCI bus transaction."

I. Respecting the "PCI bus transaction" phrase, the district court made three errors.

First, the district court erred procedurally by refusing to consider ACQIS's claim construction arguments as untimely. ACQIS's arguments were timely raised at the first opportunity in response to a new issue *EMC* first raised at summary judgment.

Second, the district court erred on the merits by misconstruing "PCI bus transaction" to require physical layer signals, including "control" signals and "parity" bits. The ordinary meaning of that phrase (in light of the full intrinsic and extrinsic record) is the information required by the PCI Specification's transaction layer (*e.g.*, address, data, command, and byte enables), not physical layer signals. EMC's systems infringe because they send the transaction layer information required by the claims.

Third, the district court erred by granting summary judgment against the Address and Data Claims based on its construction of "PCI bus transaction." Because those claims recite transmitting only the "address and data bits" of the transaction rather than an entire transaction, they cannot reasonably be read to require transmitting physical layer "control" and "parity" signals. Yet, the district court granted summary judgment of non-infringement against these claims on the basis that the accused products do not send "control" and "parity" signals. This was error.

The Court should correct the district court's construction and reverse its grant of summary judgment at a minimum, it should remand for the district court to evaluate those arguments in the first instance.

II. This Court should also clarify the district court's constructions of "communicating … a PCI bus transaction" and "encoded … (PCI) bus transaction" by giving each of these phrases its ordinary meaning in light of the construction of "PCI bus transaction."

The district court construed "communicating … a PCI bus transaction" based on a purported agreement about the meaning of that term, even though it has become clear that the parties had not actually agreed. In particular, the parties assigned materially different meanings to "control bits" in the construction. The Court should correct the error.

Finally, the district court misconstrued "encoded … (PCI) bus transaction" based on its incorrect holding that ACQIS had disavowed any meaning that did not require converting parallel signals.

Although neither of these constructions formed the basis of summary judgment, clarifying them now would be in the interest of judicial economy because the issues created by those erroneous constructions are likely to become important on remand.

ARGUMENT

I. Standard of Review

"This court reviews summary judgment decisions under the law of the regional circuit." *Momenta Pharm., Inc. v. Teva Pharm. USA Inc.*, 809 F.3d 610, 614–15 (Fed. Cir. 2015). The First Circuit reviews summary judgment grants *de novo*, reversing "if, after reviewing the facts and making all

inferences in favor of the non-moving party ..., the evidence on record is sufficiently open-ended to permit a rational factfinder to resolve the issue in favor of either side." *Adamson v. Walgreens Co.*, 750 F.3d 73, 78 (1st Cir. 2014).

"[T]he ultimate issue of the proper construction of a claim should be treated as a question of law." *Teva Pharm. USA, Inc. v. Sandoz, Inc.*, 574 U.S. 318, 326 (2015). The Court reviews "subsidiary factual findings on extrinsic evidence" for clear error. *Wi-LAN USA, Inc. v. Apple Inc.*, 830 F.3d 1374, 1381 (Fed. Cir. 2016) (brackets omitted).

"[T]his court applies Federal Circuit precedent when determining whether a claim construction argument has been waived." *Lazare Kaplan Int'l, Inc. v. Photoscribe Techs., Inc.*, 628 F.3d 1359, 1376 (Fed. Cir. 2010). Issues of "waiver for failure to timely present evidence or raise an issue[] are reviewed for abuse of discretion." *F.lli De Cecco di Filippo Fara S. Martino S.p.A. v. United States*, 216 F.3d 1027, 1031 (Fed. Cir. 2000). "A district court abuses its discretion when its decision is based on clearly erroneous findings of fact, is based on erroneous interpretations of the law, or is clearly unreasonable, arbitrary or fanciful." *Whitserve, LLC v. Comput. Packages, Inc.*, 694 F.3d 10, 26 (Fed. Cir. 2012).

II. Granting summary judgment based on an incorrect construction of "PCI bus transaction" was error.

The district court misinterpreted its earlier claim construction of "PCI bus transaction." Appx6–11. ACQIS does not dispute the district court's original construction of that term—*i.e.*, "a transaction, in accordance with the … PCI Local Bus Specification." Appx3. ACQIS does, however, dispute the district court's reinterpretation of that construction at summary judgment—*i.e.*, its holding that "in accordance with the … PCI Local Bus Specification" means communicating physical layer "control" and "parity" signals. Appx7–8. That is not what the specification requires.

That reinterpretation resulted from procedural and substantive errors. Appx6–11. The district court erred *procedurally* by refusing to consider ACQIS's claim interpretation arguments as purportedly untimely and therefore waived. Appx9–10. It erred *substantively* by construing a "PCI bus transaction" to require physical layer "control" and "parity" signals.

The Court should hold that "a transaction, in accordance with the … PCI Local Bus Specification" need not include physical layer signals, or in the alternative, remand with instructions for the district court to consider ACQIS's arguments in the first instance.

A. ACQIS's arguments were timely.

The district court refused to consider ACQIS's arguments regarding the reinterpretation of "PCI bus transaction" urged by EMC on the

erroneous basis that ACQIS's arguments were "untimely" and therefore waived. Appx9–10. Far from untimely, the arguments arose in a routine pre-trial dispute over interpretation of a previously issued claim construction—a dispute that *EMC*, not ACQIS, had raised unexpectedly at summary judgment. ACQIS responded immediately in its opposition with arguments consistent with positions it had taken for years. ACQIS's arguments were therefore timely and not waived. This Court should vacate the grant of summary judgment and remand for the district court to consider ACQIS's claim construction arguments in the first instance.

1. EMC, not ACQIS, raised a new claim construction position at summary judgment.

To start, the district court wrongly characterized the claim construction dispute as manufactured by ACQIS at summary judgment. To the contrary, *EMC* first raised the dispute at summary judgment, not ACQIS. Appx1734–1736.

Before summary judgment briefing, the parties did not debate whether "transaction" refers to physical layer signals. But that was because ACQIS had argued for years that "transaction" did not include such signals, and EMC had not clearly objected.

a) ACQIS argued for years that a "PCI bus transaction" is defined by transaction layer data.

Throughout this litigation, ACQIS maintained that a "PCI bus transaction" is defined by the PCI Specification's *transaction layer*, and not by its physical layer.

1. Before Judge Davis, ACQIS maintained that a "'PCI bus transaction' is best described as 'digital *command, address, and data information*, in accordance with the PCI standard"—*i.e.*, the transaction layer information—"because according to the PCI specification, that is what makes up a PCI bus transaction." Appx484 (emphasis added); *see also* Appx484 n.4 ("the thing that determines whether the devices … convey a PCI bus transaction, is the information—the command, address, and data information in accordance with the PCI standard"); Appx394 (the "intrinsic evidence all consistently require a 'bus transaction' of the PCI standard to require 'command, address, and data information'"); Appx390–395.

2. Before the Board, ACQIS again maintained that a "PCI bus transaction" is the "command, address, and data information, in accordance with the PCI standard." Appx679, Appx673–685.

3. Before the district court, ACQIS again argued that a "transaction, in accordance with the industry standard PCI Local Bus Specification" was the "address, command, and data information [required] in accordance with the PCI Standard." Appx1160, Appx1170. At the *Markman* hearing, ACQIS

confirmed that "the characteristics of a PCI bus transaction" are a "PCI address," "command code," and the "data"—*i.e.*, the transaction layer data. Appx1540–1541 (125:7–126:2).

ACQIS argued explicitly that a "transaction" does *not* refer to physical layer signals. In its claim construction briefing, ACQIS stated that the inventor "chose to keep the information contained in the transaction layer of the PCI protocol, *but eliminate the physical layer of that protocol*." Appx1159 (emphasis added). At the *Markman* hearing, ACQIS explained that a "PCI bus transaction" "has to involve the transaction layer," "not the physical bus." Appx1560 (145:22–25).

ACQIS had also consistently argued that the accused devices infringe because they communicate "PCI addresses," "command instructions," and "data." Appx1544 (129:17–130:2); *see also* Appx1546 (131:23–132:1) ("the PCI drivers read, not surprisingly, PCI addresses. They read PCI command information, and then they work and exchange the data as is required by the protocol"); Appx1554 (139:9–12) (arguing that a PCI driver must understand "a PCI address … PCI command information … and … data."); Appx1555 (140:3–141:14) (detailing the address, command, and data exchanged during a "transaction").

Accordingly, ACQIS argued consistently for years that a "PCI bus transaction" is a transaction as defined by the transaction layer of the PCI Specification, and that physical layer signals are irrelevant.

b) EMC did not clearly object to ACQIS's manifest understanding.

At no point during the claim construction proceeding did EMC clearly object to ACQIS's repeated statements that a "PCI bus transaction" is defined only by transaction layer information. To the contrary, EMC appeared to *agree*. *Compare* Appx1126 (EMC arguing that a "transaction" "is an active exchange of something (*e.g.*, an exchange of information) between two or more entities") *with* Appx1205 (¶ 61) (ACQIS's expert opining that "a 'transaction,' within the context of the PCI standard and the patents, is an exchange of information between interconnected computer components"). Rather than speak out about any dispute on this issue at claim construction, EMC emphasized instead that "the only issue that we believe is remaining on this point is whether or not the PCI bus transaction has to involve a PCI bus." Appx1480 (65:16–19); *see also* Appx1443 (28:19-20); Appx1382–1383. Judge Davis's decision that the claims do not require a PCI bus then was not disturbed.

Hints of EMC's eventual summary judgment position can only be divined in hindsight. For example, when discussing a different term ("control bits"), EMC noted (in a parenthetical) that those bits "control the timing of events on the PCI bus"—perhaps implying that physical layer signals may be relevant to "control bits." Appx1138. EMC made a similar drive-by at the *Markman* hearing. Appx1527 (112:18–19) (mentioning in an

aside that "[c]ontrol bits actually control the sequencing of the transaction"). But EMC never squarely confronted ACQIS's repeated and manifest understanding that a "PCI bus transaction" is the transaction-layer information exchanged by PCI components.

It was not until summary judgment that EMC unexpectedly challenged that position. ACQIS timely responded that EMC's reinterpretation of the district court's construction constituted an "improper narrowing [that] is inconsistent with the Court['s claim construction] ruling that no physical PCI Local Bus is required." Appx3348. ACQIS's position was consistent with what it had argued for years. It was therefore wrong to criticize ACQIS for failing to recognize, let alone preemptively respond to, EMC's new argument before EMC ever raised it.

Importantly, the district court did not hold that ACQIS's claim construction arguments prejudiced EMC or that ACQIS was otherwise estopped from making them. Indeed, it could not have done so because ACQIS had taken the same position for years—*i.e.*, that a "transaction" requires only transaction layer information. It was therefore timely for ACQIS to reassert its position in response to EMC's unanticipated reinterpretation of the district court's construction, and wrong of the district court to conclude otherwise.

2. A claim construction dispute arising at summary judgment is timely.

Even if ACQIS *could have* theoretically anticipated and raised EMC's claim construction dispute earlier, that possibility would still not justify a finding of waiver because ACQIS nevertheless raised the dispute *pre-trial*, and ACQIS's arguments were consistent with its positions throughout the litigation. The district court's contrary holding was an abuse of discretion because it was "based on erroneous interpretations of the law." *Whitserve*, 694 F.3d at 26.

"[A] district court may engage in claim construction during various phases of litigation, not just in a *Markman* order." *Conoco, Inc. v. Energy & Envtl. Int'l, L.C.*, 460 F.3d 1349, 1359 (Fed. Cir. 2006). That includes making claim construction rulings "on summary judgment … rather than in the phase of the case specifically dedicated to claim construction." *Wi-LAN USA*, 830 F.3d at 1381. Moreover, a "district court may (and sometimes *must*) revisit, alter, or supplement its claim constructions … to the extent necessary to ensure that final constructions serve their purpose of genuinely clarifying the scope of claims for the finder of fact." *In re Papst Licensing Digital Camera Patent Litig.*, 778 F.3d 1255, 1261 (Fed. Cir. 2015) (emphasis added); *see also Jack Guttman, Inc. v. Kopykake Enters., Inc.*, 302 F.3d 1352, 1361 (Fed. Cir. 2002) (a district court may "revisit[] and alter[] its interpretation of the claim terms"). "This is particularly true where

issues involved are complex, either due to the nature of the technology or because the meaning of the claims is unclear from the intrinsic evidence." *Guttman*, 302 F.3d at 1361.

Accordingly, district courts routinely revise constructions—before or even during trial—when disputes arise. *See*, *e.g.*, *Intervet Inc. v. Merial Ltd.*, 617 F.3d 1282, 1289 (Fed. Cir. 2010) (holding that the district court incorrectly interpreted its earlier construction at summary judgment); *Moba, B.V. v. Diamond Automation, Inc.*, 325 F.3d 1306, 1313 (Fed. Cir. 2003) (per curiam) (hearing a dispute over the district court's interpretation of its earlier claim construction); *Gen. Surgical Innovations, Inc. v. Origin Medsystems, Inc.*, 250 F.3d 761, 2000 WL 959507, at *3 (Fed. Cir. 2000) (table) ("[a]lthough neither party appeals the district court's construction … the parties disagree as to the interpretation of the district court's claim construction").

In *Intervet* (as here) the district court issued a *Markman* order construing a disputed term. 617 F.3d at 1289. And, as here, the district court granted summary judgment of non-infringement based on interpretation of that earlier construction. *Id.* The appellant disputed only the subsequent *interpretation* of that construction. *Id.* This Court agreed that the interpretation was "inconsistent with the district court's otherwise correct [original] claim construction," "reverse[d] the district court's claim construction[]," "clarif[ied] the proper interpretation of the construction,"

and "remand[ed] the question of infringement for a determination consistent with the claim constructions articulated" by the Court. *Id.* at 1289–90.

The fact pattern here is similar. The district court had construed a "PCI bus transaction" as "a transaction, in accordance with the … PCI Local Bus Specification…." Appx1703–1704. Defining that term with reference to the "PCI Local Bus Specification" left open exactly what information was "in accordance with" that Specification.

At summary judgment, EMC argued that a transaction is "in accordance with" the PCI Specification only if it includes certain physical layer signals defined in that specification. Appx1734–1736. ACQIS timely disagreed in its opposition (Appx3347–3359) and accompanying expert declaration (Appx3394–3420), explaining why a person of ordinary skill would not have understood a "transaction, in accordance with the … PCI Local Bus Specification" to include the physical layer signals EMC identified. Appx3342, Appx3347–3359.

There was nothing unusual about this routine sequence. As in *Intervet*, a pre-trial dispute over the meaning of an earlier construction arose during summary judgment. As EMC wrote at the time, "the only dispute here … is a pure legal issue of claim construction." Appx1743. And "[w]hen the parties present a fundamental dispute regarding the scope of a

claim term, it is the court's duty to resolve it." *O2 Micro Int'l Ltd. v. Beyond Innovation Tech. Co.*, 521 F.3d 1351, 1362 (Fed. Cir. 2008).

But the district court here did not. Instead, it refused to resolve the dispute, dismissing ACQIS's arguments as "untimely" because it believed "district courts are not obligated to rule on claim construction arguments presented for the first time in summary judgment briefs." Appx9–10 (citing *Function Media, L.L.C. v. Google Inc.*, 708 F.3d 1310, 1325 (Fed. Cir. 2013)). Those are errors of law.

"[L]itigants waive their right to present new claim construction disputes if they are raised for the first time *after trial*." *Conoco,* 460 F.3d at 1359 (emphasis added); *see also Broadcom Corp. v. Qualcomm Inc.*, 543 F.3d 683, 694 (Fed. Cir. 2008) (same). Accordingly, district courts routinely hear arguments and resolve claim construction disputes that arise as late as the close of evidence. *Eli Lilly & Co. v. Aradigm Corp.*, 376 F.3d 1352, 1360 (Fed. Cir. 2004) (a party waives a claim construction issue raised for the first time "[o]nly after the presentation of all of the evidence to the jury"). (Of course, here, the dispute was *before* trial.)

Thus, for example, it made no difference in *Intervet* "that at the time of the *Markman* hearing, [appellant] did not see any" problem with the original claim construction. 617 F.3d at 1289. What mattered was that a material dispute arose about that construction *pre-trial*. Contrary to the district court's holding here, it was not incumbent on ACQIS to have

anticipated the dispute back at the claim construction phase and to have "tee[d] up a summary judgment position based on a particular construction" that EMC had not previously advanced. Appx9–10.

The district court was also wrong as a matter of law in holding that "district courts are not obligated to rule on claim construction arguments presented for the first time in summary judgment briefs." Appx10. Indeed, the case the court cited for that proposition (*Function Media*) holds the opposite. In *Function Media*, this Court found *no* waiver because the claim construction dispute "was brought to the district court's attention *during trial* and the court heard arguments from both sides." *Function Media*, 708 F.3d at 1325 (emphasis added). Accordingly, *Function Media* does not support the district court's conclusions that ACQIS's arguments were untimely and that the it had no obligation to hear them.

None of the other authority the district court cited supports that conclusion either. *ePlus, Inc. v. Lawson Software, Inc.* simply held "that a *post-trial* challenge" to claim construction is "inappropriate and untimely," Appx10 (citing 700 F.3d 509, 520 (Fed. Cir. 2012)) (emphasis added), but ACQIS's arguments were not made post-trial, but at summary judgment. Accordingly, *ePlus* does not support the district court's conclusion either.

The district court cited *O2 Micro* for the proposition that district courts are not "required to construe *every* limitation present in a patent's asserted claims." Appx10 (citing 521 F.3d at 1360–62). But ACQIS's

arguments concerned a dispositive claim construction dispute, "not an obligatory exercise in redundancy." *O2 Micro*, 521 F.3d at 1362. As *O2 Micro* held, "[w]hen the parties present a fundamental dispute regarding the scope of a claim term, it is the court's duty to resolve it." *Id.*

Simply put, the district court got the law wrong. And because its waiver holding was "based on erroneous interpretations of the law," it was an abuse of discretion. *Whitserve*, 694 F.3d at 26. Accordingly, if this Court does not reach the merits and reverse, it should at a minimum vacate the grant of summary judgment and remand to the district court to evaluate ACQIS's claim construction arguments and uncontradicted evidence in the first instance. On remand, the district court should consider those legal arguments as well as "any appropriate recourse to extrinsic evidence concerning the usage and understanding of the term ['PCI bus transaction'] in relevant context," including the expert declarations ACQIS submitted. *Verve, LLC v. Crane Cams, Inc.*, 311 F.3d 1116, 1120 (Fed. Cir. 2002).

B. The district court erred by holding that a "transaction, in accordance with" the PCI Specification must include physical layer "control" and "parity" signals.

If the Court determines that the record on appeal is sufficiently developed, it should reach the merits and hold that a "transaction, in accordance with the … PCI Local Bus Specification" does not include the physical layer signals on which summary judgment was based.

The parties and the district court all agreed that the claims use the phrase "PCI bus transaction" to refer to information that defines a "transaction, as defined by … the PCI Local Bus Specification." Appx1700. The dispute is whether a skilled artisan would have understood the term "transaction" as referring to the transaction layer information defined in that standard (as ACQIS argued) or instead as also encompassing certain physical layer signals (as EMC argued and the district court accepted). The record supports only ACQIS's interpretation.

"[C]laim construction must begin with the words of the claims themselves." *In re Power Integrations, Inc.*, 884 F.3d 1370, 1376 (Fed. Cir. 2018). The Court then considers the intrinsic evidence, which here includes the written description, the prosecution history, and the PCI Specification.[5] *Phillips v. AWH Corp.*, 415 F.3d 1303, 1315 (Fed. Cir. 2005). Finally, "resolution of any ambiguity arising from the claims and specification may be aided by extrinsic evidence." *Verve*, 311 F.3d at 1119–20.

Here, the evidence demonstrates that "PCI bus transaction," as used in the claims, refers to the transaction layer information defined by the PCI Standard.

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[5] The PCI Specification is intrinsic evidence because it is cited on the face of at least one patent in each of the three asserted patent families. *Kumar v. Ovonic Battery Co.*, 351 F.3d 1364, 1368 (Fed. Cir. 2003) ("prior art cited in a patent or cited in the prosecution history of the patent constitutes intrinsic evidence").

1. Claim language.

Nothing in the claim language suggests that a "PCI bus transaction" includes physical layer control and parity signals. None of the asserted claims recites that a "transaction" includes such physical layer signals. Neither do any of the unasserted claims.

In contrast, several asserted claims *do* recite that the "transaction" includes *transaction layer* information, such as "address and data bits of [a] (PCI) bus transaction" or the "data bits of [a] PCI bus transaction." '171 patent (cl. 24) (Appx332); '468 patent (cl. 29); (Appx372) '119 patent (cl. 38) (Appx293); '814 patent (cl. 31) (Appx246). The claim language therefore suggests that a "transaction" includes transaction layer information (*e.g.*, address and data bits) but not physical layer signals.

The district court's holding that the claims do not require a PCI Local Bus also supports ACQIS. Appx1700–1704. It is undisputed that the physical layer signals on which summary judgment rests "are only used to facilitate communication over a physical PCI Local Bus." Appx3396, Appx3403 (¶¶ 15, 38) (ACQIS's expert declaration); *see also* Appx3398 (¶ 24) ("interface control signals are a requirement specific to communication of a transaction over a physical PCI Local Bus"). In other words, a person of skill would know that physical layer signals are only needed if a physical PCI Local Bus is. With no physical PCI Local bus required, no physical layer signals would be required either.

Given the district court's holding that the claims include embodiments with no PCI Local Bus, it makes no sense to then construe the claims to read back useless physical layer signals. Simply put, because the claims require no PCI Local Bus, a skilled artisan would have understood that they require no physical layer signals to control a non-existent PCI Local Bus. Appx3400 (¶ 30).

2. Intrinsic record

The intrinsic record demonstrates that "PCI bus transaction" does not include physical layer control and parity signals. That record contains both (1) the patent specifications and (2) the PCI Specification.

a) Patent specifications

The patent specifications, like the claim language, disclose embodiments that *exclude* the PCI Local Bus and therefore have no use for physical layer signals. For example, as shown in Figure 8 of the '415 Patent, PCI components connect directly to interface controllers, or through other bus types, *without any intervening PCI Local Bus*. In the context of such embodiments, it would be illogical to read into the claimed requirement of communicating a "PCI bus transaction" any PCI *physical layer* signals.

Moreover, the specifications *also* describe embodiments where components connect to the interface controllers using a PCI Local Bus. *See*, *e.g.*, Appx24 (Figure 7). And in those embodiments, interface controllers use

separate hardware to capture and convey physical layer signals coming across that PCI Local Bus. *See*, *e.g.*, Appx43–44 (16:63-17:54).

This disclosure implies that the physical layer signals are *not* present in *all* embodiments, contrary to the district court's construction. As described above, where an interface controller receives a "PCI bus transaction" directly from a processor or from an "other bus," without any intervening PCI Local Bus, it would make little sense to understand the term "PCI bus transaction" as denoting physical layer signals for controlling the non-existent bus. But the district court's construction does exactly that.

Take oral conversations. Communicating a "PCI bus transaction" is analogous to communicating a "conversation." Embodiments that communicate the conversation from one telephone network to another (analogous to embodiments that communicate a "PCI bus transaction" from one PCI Local Bus to another) would communicate both the conversation *and* the signals necessary to control the telephone networks. But embodiments that communicate the conversation over a different physical medium would naturally not communicate signals necessary to control a telephone network, because no telephone network exists in those embodiments. Thus, if a claim term applied to both embodiments such as "telephone conversations," it would make little sense to interpret its instruction to communicate a "telephone conversation" as requiring communicating signals necessary to control a telephone network.

The patent specifications further confirm this understanding by disclosing that, where physical layer PCI signals exist, they are processed separately from the transaction layer information. *Id.* (17:16–54) (processing the transaction layer "address and data information" by encoders 1022 and 1027 and processing physical layer signals by "control encoder & merge data path unit 1025").

b) PCI Specification

The PCI Specification also confirms that "PCI bus transaction" does not refer to physical layer data, but to transaction layer data. It does so both by (1) defining a "transaction" by reference to the transaction layer data exchanged between components, and (2) repeatedly describing the physical layer signals as separate from the "transaction."

First, the PCI Specification defines a "transaction" by reference to the transaction layer information, not physical signals. In particular, the PCI Specification defines a "transaction" as "an address phase plus one or more data phases," with an "address phase" defined as "a single address transfer," and a "data phase" as a "transfer state" "in which [the] data is transferred" ("plus zero or more wait states"). Appx2357–2358; Appx3396–3397 (¶¶ 17–18). The PCI specification thus defines a "transaction" in terms of the information actually transferred between the master and target components, not in terms of physical layer signals never received into the memory of the devices communicating over the bus. Appx3400 (¶ 29) ("the

interface control signals are not received in the memory of the devices communicating over the bus, thus, they are not part of the transaction").

Second, the PCI Specification repeatedly describes the physical layer signals on which the district court relied as separate from the "transaction." For example, its glossary describes various physical layer control signals as separate from the "transaction"—*e.g.*, the DEVSEL# signals as "allow[ing] a target to claim a transaction," and the FRAME# signal as "defining the boundary of the transaction." Appx2355; *see also* Appx3400 (¶ 28). As such, these control signals are not part of the transaction.

The same is true of the "parity signal." Appx3403–3404 (¶¶ 37–45). The parity bit is calculated to confirm that the *transaction layer* information was transmitted correctly—*i.e.*, is "calculated from the address, data, command, and byte enable bits." Appx3403 (¶ 40); *see also* Appx2332. Accordingly, "the parity bit itself provides a *transport* function and is not part of the transaction." Appx3403 (¶ 37) (emphasis added). Thus, the PCI Specification consistently describes the parity bit as something separate from the transaction. For example, it discloses that the parity signal "provides a mechanism to determine *transaction by transaction* if the master is successful in addressing the desired target and if data transfers correctly between them." Appx2332; *see also* Appx3403 (¶ 39). The PCI Specification describes the parity bit as "lag[ging] the corresponding address or data by one clock." Appx2332; *see also* Appx3404 (¶ 42). "In other

words, parity is sent *after* the transaction." Appx3404 (¶ 42) (emphasis added). Thus, a parity signal is not part of the transaction, but separate and sent only after transmission of the transaction to which it pertains to confirm correct transmission of that transaction.

3. Extrinsic record

The extrinsic evidence confirms that the ordinary meaning of a "PCI bus transaction" is the transaction layer information defining a PCI operation, and not physical layer signals. Appx3396–3400, Appx3403–3404 (¶¶ 16-31, 37–45).

Expert testimony submitted by ACQIS established that the ordinary meaning of "'transaction,' within the context of the PCI Standard and the patents, is an exchange of information between interconnected computer components," and not physical layer signals. Appx1205 (¶ 61). Expert testimony establishes that a transaction would mean the message, not its messenger:

> A person of ordinary skill would understand a "transaction" as the data exchanged over a connection, that is, the message communicated and not the messenger that delivers the message. A person of ordinary skill would not consider a particular physical layer, or the control signals necessary for sending information over a particular type of physical layer, to be part of the transaction. Rather, the "transaction" is the information exchange that occurs over a given physical interface, specifically in the case of the PCI Local Bus Specification, writing data to,

> or reading data from a particular memory location defined by the specification.

Appx2471 (¶ 52).

Expert testimony confirms that a person of ordinary skill would have understood the PCI Specification as using the term "transaction" consistently with this ordinary meaning. Appx3397 (¶ 19) ("the PCI Local Bus Specification defines a transaction as the information communicated in the address phase and data phase;" parity signals are sent in a later phase); Appx2470 (¶ 50) ("The PCI Local Bus Specification describes the information communicated over the physical layer as a 32-bit 'transaction.'"); Appx2505 (¶ 110) (a "transaction [as] defined by the PCI Local Bus Specification refers to the information conveyed" between the two PCI components for performing a PCI operation).

Finally, expert testimony establishes that, for many of the reasons already discussed, a skilled artisan would have understood the PCI Specification as treating the physical layer "control" and "parity" signals as separate from the "transaction." Appx3398–3400, Appx3403–3404 (¶¶ 23–31, 37–45).

The entire record therefore establishes that "transaction" refers to the transaction layer data communicated from one PCI component to another, and not to the physical layer signals used only to facilitate that communication.

Given this understanding, a "transaction" is "in accordance with the PCI Local Bus Specification" if it includes the transaction layer information the PCI Specification requires—typically the address, data, command, and byte enables for most types of transactions. Appx2505 (¶ 110); Appx3397 (¶ 20). Whether transactions communicated by the accused systems are "in accordance with" the PCI Specification is the factual question of infringement. If factual disputes remain, a jury should be empaneled to decide that question.

The Court should "reverse the district court's claim construction," "clarify the proper interpretation of the construction," and "remand the question of infringement for determination consistent with the claim constructions articulated" by the Court. *Intervet*, 617 F.3d at 1290. Because the court's non-infringement analyses respecting the "communicating" and "encoded" limitations were based entirely on its erroneous interpretation of "PCI bus transaction," resolution of this issue would also require it to reevaluate those analyses.

C. The district court's construction does not preclude infringement of the Address and Data Claims.

Even if the district court had correctly interpreted "PCI bus transaction" to require the physical layer control and parity signals (it did not), this still would not justify summary judgment of non-infringement against the Address and Data Claims because those claims recite explicitly

that only the "address and data bits of [that] … PCI bus transaction" are communicated.[6] Because the accused products indisputably transmit those recited bits, the district court erred in granting summary judgment of non-infringement with respect to those claims.

As ACQIS argued repeatedly to the district court (Appx3337–3338; Appx1178; Appx1226 ¶ 129; Appx1635–Appx1636 (220:15–221:6); Appx1393), the Address and Data Claims "state precisely what must be communicated: *only* the "address and data bits of a PCI bus transaction." Appx3337 (emphasis added). For example, claim 31 of the '814 patent recites that the peripheral bridge "communicate[s] *address and data bits of [a] PCI bus transaction* in serial form over said second LVDS channel." Appx246 (cl. 31) (emphasis added). Accordingly, even if a "PCI bus transaction" were to include, as the district court held, physical layer control and parity signals, the requirement of transmitting only the "address and data bits of [a] PCI bus transaction" would clearly not require also transmitting these physical layer control and parity signals.

For purposes of summary judgment, EMC accepted that the accused products communicate all address and data bits. Appx1764 n.26. ACQIS argued that this admission foreclosed summary judgment on the Address

[6] '171 patent (cl. 24) (Appx246); '468 patent (cl. 29) (Appx372); '814 patent (cl. 31) (Appx246); '119 patent (cl. 38) (Appx293).

and Data Claims because those claims only required communicating the address and data bits. Appx3337, Appx3338. The district court ignored the argument and granted summary judgment of non-infringement against those claims anyway. For this additional, independent reason, the Court should reverse the grant of summary judgment and remand for trial on infringement of at least the Address and Data Claims.

III. The Court should correct the district court's constructions of "communicating" and "encoded."

Though the district court briefly discussed "communicating … [a] PCI bus transaction" and "encoded … (PCI) bus transaction," its non-infringement analysis of each turned entirely on its interpretation of "PCI bus transaction." Specifically, the district court held that, because the accused products lack a "PCI bus transaction," they can neither "communicate a PCI bus transaction" nor "encode[] … [a] (PCI) bus transaction" regardless of what "communicating" or "encoded" mean. Appx3, Appx11–13.

For example, the district court's only analysis of the "communicating" phrase was to note that it had "already concluded that the claims are limited by the Specification" and that summary judgment was appropriate "for the reasons described above." Appx12–13. Its analysis of the "encoded" term also turned only on its construction of "PCI bus transaction": it held that "ACQIS asserts that EMC's products modify *some data* from parallel to

serial form prior to communicating or transacting that data, but ACQIS does not actually identify a *PCI bus transaction* that is converted from parallel to serial form and communicated by the accused products." Appx12. Accordingly, the Court can reverse the entire summary judgment order by correcting or vacating the construction of "PCI bus transaction" alone.

Nevertheless, as this Court has explained, "[i]n the interest of judicial economy, we have the discretion to review a non-dispositive claim construction if we believe that the construction may become important on remand." *Interval Licensing LLC v. AOL, Inc.*, 766 F.3d 1364, 1376 (Fed. Cir. 2014); *see also Lexington Luminance LLC v. Amazon.com Inc.*, 601 F. App'x 963, 970 (Fed. Cir. 2015). The Court has exercised that discretion where, for example, the disputed claim term appears in claims for which the court was vacating summary judgment of non-infringement. *Interval Licensing*, 766 F.3d at 1376 ("Because we are vacating the judgment of non-infringement as to claims 15–18 of the '652 patent, and because those claims include the [disputed] term 'instructions,' we take this opportunity to address the claim construction of that term.").

The Court should exercise its discretion here and hold that "communicating … [a] PCI bus transaction" and "encoded … (PCI) bus transaction" carry their ordinary meanings, in view of the ultimate construction of "PCI bus transaction." The ordinary meaning is simply to convey code representing a PCI bus transaction, and ACQIS will prove at

trial that EMC's accused systems do just that. Moreover, revising those constructions is necessary because the district court (1) wrongly construed the "communicating" phrase pursuant to an apparent but illusory agreement between the parties, and (2) wrongly construed the "encoded" phrase based on an erroneous finding of prosecution disclaimer.

A. "Communicating … [a] PCI bus transaction" should be given its ordinary meaning.

As ACQIS argued below (Appx1177; Appx1711), "communicating … [a] PCI bus transaction" carries its ordinary meaning in light of the construction of "PCI bus transaction." At the *Markman* hearing, ACQIS consented to EMC's proposal that this meaning was "communicating a PCI bus transaction, including all address, data, and control bits." Appx1711–1712.

Unfortunately, as now apparent, the parties assigned materially different meanings to the term "control bits." ACQIS made it clear that it understood that term as it always had—*i.e.*, the transaction layer's command and byte enable bits (which the accused products communicate)—whereas EMC claimed at summary judgment that the phrase referred to the physical layer's interface control signals (which EMC says the accused products do not communicate). Appx1725.

Because the court's construction of "communicating … [a] PCI bus transaction" was adopted based on EMC's version of the agreement—a

version that was inconsistent with what ACQIS made clear it was agreeing to, it should be vacated. The Court should then hold that the phrase carries its ordinary meaning in light of the Court's resolution of the "PCI bus transaction" phrase, or alternatively, remand for the district court to consider the issue in the first instance.

Relief is appropriate here because the disagreement over the meaning of "control bits" is genuine and timely. When ACQIS agreed to construe "communicating … [a] PCI bus transaction" as communicating "all the address, data, and *control bits*," it made explicit that it understood "control bits" to mean command information:

> THE COURT: If I took their definition and deleted like the last six words, you'd be okay with that?
>
> MR. BROGAN: … I think that's right. Because I think you would communicate, in a PCI bus transaction you do communicate the address, **you do communicate a command that tells you what you have to do** and then you send the data. So I think that's right. That's all right.
>
> …
>
> And if you have no PCI address and no **command** that tells you what transaction is going to take place, you can't say that's a PCI bus transaction.
>
> …
>
> If you only have some of the bits and you don't have a **command**, then you wouldn't be able to carry out a PCI bus transaction.

Appx1642–1643 (227:25–228:15) (emphasis added).

ACQIS's understanding was no surprise because the phrase "control bits" is used in the art to refer to the transaction layer's command and byte enable bits (Appx2473 (¶ 57); Appx3419–3420 (¶ 83)), and both ACQIS and had used it that way throughout the litigation.

For example, at the IPR hearing, ACQIS represented that "control bits" describe the PCI *command*. *See*, *e.g.*, Appx1034–1035 (describing "address and the *control bits*" indicating the type of *command*, such as "interrupt acknowledge") (emphasis added). To remove any confusion, ACQIS told the district court explicitly at the *Markman* hearing that it had used the term "control bits" in the IPR hearing to "refer[] to the command." Appx1641 (226:12–15).

ACQIS's expert (Dr. Gafford) had also used the term "control bits" in his reports to refer to command bits and byte enables. *E.g.*, Appx2601 (¶ 243) (expert report). And at his deposition, he too clarified that that he used "control bits" to refer to the command and byte enables. Appx2158 (457:8-10) ("Q: And by control bits, you're referring to command and byte enables; correct? A: That's right.").

Throughout the *Markman* hearing, ACQIS also used "control bits" to refer to the transaction layer's command information and byte enables. *E.g.*, Appx1629 (214:14–16) ("a PCI bus transaction that's defined by the standard. You know the three portions, address, data and control. So those things that tell you what it is that you're going to do when you exchange the

information."); Appx1641 (226:12–15) ("'That includes data, that includes address except for interrupt acknowledge, and that includes the control bits.' He says every time. He's referring to the command.").

Even *EMC* used "control bits" to refer to command and byte enable information. For example, at the *Markman* hearing, EMC argued that ACQIS's expert had agreed "with no ambiguity" that "*control bits*" must be communicated. Appx1533 (118:10–119:23) (emphasis added). To show this agreement, EMC pointed to deposition testimony where ACQIS's expert had agreed that "*command information and byte enable[s]*" must be communicated. Appx1533 (118:10–119:23) (emphasis added). EMC thus equated "control bits" with "command information and byte enables," even at the *Markman* hearing.

EMC never disputed ACQIS's statements equating "control bits" with command and byte enables. Just the opposite. When ACQIS agreed that "communicating … [a] PCI bus transaction" requires communicating "control bits," it stated expressly that this was "all right" only if "control bits" referred to "command bits." Appx1643 (228:2–15). Rather than object, EMC took a short recess, and upon returning, simply declared that "we're comfortable proceeding with the construction to which [ACQIS's counsel] agreed," thus acquiescing in ACQIS's position. Appx1645 (230:10–13).

At summary judgment, EMC unexpectedly revealed that it interpreted "control bits" to mean *physical layer* control signals. Appx1765.

When ACQIS reiterated that "control bits" refers to command and byte enables (Appx3338, Appx3373–3376; Appx3417–3420 (¶¶ 75–83)), EMC responded with indignance to what it called "the fiction that the Court actually construed 'control bits' to mean command and byte enable bits." Appx3457.

It was not a fiction. It was what ACQIS explicitly had agreed to. And given ACQIS's other arguments throughout the litigation and the *Markman* hearing—*i.e.*, that a "PCI bus transaction" "has to involve the transaction layer" and "not the physical bus" (Appx1560 (145:22–25); *see also supra* § I.A.1)—it would have been impossible to reasonably interpret ACQIS's agreement on "control bits" as an agreement that physical layer signals are required.

In any event, it has become clear that the district court adopted a materially ambiguous construction of "communicating … [a] PCI bus transaction," based on a purported agreement between the parties that in fact never existed. To avoid further confusion, the Court should either vacate the construction and hold that the phrase carries its ordinary meaning in light of "PCI bus transaction," as ultimately construed, or, in the alternative, remand for the district court to construe the phrase in the first instance.

B. ACQIS made no disavowal requiring an "encoded … (PCI) bus transaction" to be serialized from parallel signals.

The Court should vacate the erroneous construction of "encoded … (PCI) bus transaction." Appx1704–1711. Judge Davis construed "encoded … PCI bus transaction" to simply mean "code representing a PCI bus transaction." Appx508. The district court revised that construction to a "transaction that has been serialized *from a parallel form*," based on EMC's false narrative that ACQIS had "defeat[ed] the IPRs" by disavowing broader claim scope. Appx1704–1711; Appx1137. But "for prosecution disclaimer to attach, [Federal Circuit] precedent requires that the alleged disavowing actions or statements made during prosecution be both clear and unmistakable." *Omega Eng'g, Inc. v. Raytek Corp.*, 334 F.3d 1314, 1325–26 (Fed. Cir. 2003) (noting also that "[a]mbiguous language cannot support disavowal"). That is not the case here.

At the IPR, ACQIS never distinguished the prior art based on conversion of parallel signals. The district court was led astray by EMC's false narrative, cherry-picked citations to the IPR hearing, and the court's own misunderstanding that "serialization" (*i.e.*, formatting data for serial transmission) requires the data to start as *parallel* signals rather than, for example, simply data in memory. The Court should therefore hold that

ACQIS made no disavowal, vacate the district court's order based on that finding, and hold that Judge Davis's original construction controls.

1. ACQIS never argued that "encoded" requires serializing data from parallel signals.

ACQIS did not defeat the IPRs, as EMC contends, by arguing that "encoded" requires serializing data from parallel signals. Indeed, ACQIS had never distinguished the prior art based on the "encoded" limitation at all, let alone by arguing that the limitation required converting parallel signals. Just the opposite. ACQIS had formally asked for a broader construction and then *conceded* that the prior art met the encoded limitation based on that broader construction, without converting parallel signals.

First, ACQIS had formally asked the Board for a construction of "encoded" that did *not* require serializing parallel signals. Appx798–799. Specifically, ACQIS requested a construction that included any reversible operation that "(1) turns a signal into bits, (2) groups bits into a specified size block, or (3) orders bits onto one or more serial transmission lines." Appx799. At the very least, the second two options have no relationship to parallel signals. Accordingly, ACQIS requested a construction of "encoded … (PCI) bus transaction" that did not require the transaction to have been encoded from parallel signals. This alone should be sufficient to reverse the finding of waiver.

Second, ACQIS did not even attempt to defend the IPR based on the "encoded" limitation, let alone on the basis that "encoded" requires converting parallel signals. Just the opposite. ACQIS *conceded* that the prior art *satisfied* the "encoding" limitation *without encoding parallel signals*. Appx817. Specifically, ACQIS conceded that the prior art's "8b/9b line encoding"—which fits ACQIS's second option—satisfied the "encoded" limitation. Appx817. EMC itself characterizes that type of encoding as "not parallel-to-serial conversion" (Appx1782 (¶ 57)).

Third, both EMC and the Board accepted ACQIS's concession. Appx972–973, Appx1099–1100, Appx1104 n.4. The Board therefore held (and both parties agreed) that the prior art *satisfied* the "encoded" limitation *without* serializing parallel signals. Appx1099–1100, Appx1104 n.4.

In other words, the "encoded" limitation played no role whatsoever in defeating the IPRs, but EMC told the district court the opposite. EMC argued that "encoded" "require[s] the parallel data to be serialized" because:

> ACQIS made that representation in the IPRs when it considered it necessary to do so to differentiate the prior art in order to save its patents. Having done so—and having obtained the benefit of doing so by defeating the IPRs—ACQIS is bound (and the claims are limited) by those statements.

Appx1137. That is false.

2. The statements the district court relied on do not constitute disavowal.

To support that false narrative, EMC cited quotations from the IPR hearing suggesting that some dispute existed regarding the "encoded" term and whether it required serializing parallel signals. Appx1705–1711. In adopting that narrative, he district court (1) failed to consider the totality of the prosecution history, (2) considered certain quotations out of context and not others, and (3) mistakenly conflated "serialization"—*i.e.*, formatting for serial transmission (Appx1221 (¶ 111)—with converting the data "from a parallel form" rather than, for example, from data in memory.

First, the district court failed to consider the quotations in the context of the full prosecution history. The standard for finding prosecution disclaimer is "exacting," *Poly-Am., L.P. v. API Indus., Inc.*, 839 F.3d 1131, 1136 (Fed. Cir. 2016), and must be informed by "the 'totality of the prosecution history.'" *Comput. Docking Station Corp. v. Dell, Inc.*, 519 F.3d 1366, 1379 (Fed. Cir. 2008). "To find disavowal, [courts] must find that the specification is "both so clear as to show reasonable clarity and deliberateness, and so unmistakable as to be unambiguous evidence of disclaimer." *Openwave Sys., Inc. v. Apple Inc.*, 808 F.3d 509, 513 (Fed. Cir. 2015).

The prosecution history here includes ACQIS's formal request to construe "encoded" without encoding parallel signals *and* ACQIS's accepted

concession that the prior art teaches "encod[ing]" without that feature. That context alone renders it near impossible to find anything ACQIS may have said at the IPR hearing as having distinguished its claims from the prior art based on serializing parallel signals, let alone having done so clearly and unambiguously.

Second, the district court cited instances in which ACQIS had purportedly "reiterated the importance of parallel-to-serial conversion" (Appx1706–1708), but each was taken out of context. For example, the district court observed that counsel for ACQIS had purportedly explained that "[t]he whole point [of ACQIS's invention] is you … start with the PCI address that's in the parallel slow form, serialize it and then take it back to the PCI form at the end." Appx1706 (quoting Appx1028–1029).

Read in context, however, ACQIS was plainly not attempting to distinguish the prior art based on parallel-to-serial conversion, but based on the wholly unrelated issue of using *virtual* rather than *physical* addressing. Appx1026–1029 (29:22–32:4). The Board had asked "[w]hy do you have to have a physical address to start with," (Appx1028 (31:11–12)), and ACQIS's counsel responded that "[t]he whole point is that … [y]ou start with the [*physical*] PCI address." (Appx1028–1029). Read in this context, ACQIS was clearly not attempting to distinguish the prior art based on parallel-to-serial conversion.

Third, the district court misunderstood many of the quotations it cited because it conflated "serialized"—*i.e.*, formatted for serial transmission (Appx1221 (¶ 111))—with a supposed requirement that the data start as parallel signals. For example, the district court cited ACQIS's representations that a "key to the invention was to serialize the otherwise parallel PCI bus transactions to increase communication speeds." Appx1705–1708. But those representations imply only that ACQIS's invention communicates PCI bus transactions in serial form, not that the invention first converts the transactions from parallel signals.

The district court's apparent mistake was to conflate "serialized" with conversion "from a parallel form," but those are two separate concepts. A "serialized" PCI bus transaction is one formatted for serial transmission. The serialized data could certainly start as parallel signals (*e.g.*, those from a PCI Local Bus). But a "serialized" transaction can also be created from data in memory. Appx1221 (¶ 111) ("Serialization … also refers to operations where *a data object* is converted into a stream of bits in order to store or transmit that data"). In that case, "serialized" transaction would not be converted from parallel signals. Appx1221 (¶ 111). Consequently, ACQIS's statements that the invention transmits "serialized" PCI bus transactions does not imply that the transactions started as parallel signals.

For the reasons stated above, none of ACQIS's IPR statements about the importance of serialization represent a clear and unmistakable

disclaimer that the claims require parallel-to-serial conversion. Moreover, other record statements make clear on the totality of the record that the claims do not require serializing parallel signals. Accordingly, because ACQIS made no such disclaimer, the Court should vacate the district court's revised claim construction order and hold that Judge Davis's original construction continues to control.

As noted above, the claim construction regarding serialization of parallel signals is non-dispositive because (1) the district court did not rely on it to grant summary judgment (Appx11–12), and (2) ACQIS presented an alternative infringement theory under this construction.[7] Nevertheless, in the interests of judicial economy, the Court should reach the issue now rather than waiting to correct the error after a jury trial.

[7] Because the district court's construction of "encoded" relied on characterizing serialization from memory as "parallel-to-serial" conversion, ACQIS argued at summary judgment that the accused systems transmit "encoded" transactions at least because the transactions are serialized from memory. Appx3363; Appx3409–3410 (¶ 63).

CONCLUSION

The Court should reverse the district court's grant of summary judgment, hold that (1) a "PCI bus transaction" does not require any physical layer signals, including interface control and parity bits, and (2) "communicating … [a] PCI bus transaction" carries its ordinary meaning, and vacate the district court's construction of "encoded … (PCI) bus transaction."

Respectfully submitted,

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